In The United States Patent And Trademark Office

Applicant:	Manrique J. Brenes; Yen T. Nguyen		
Assignee:	Cisco Technology, Inc.		
Title:	METHOD AND SYSTEM FOR REAL-TIME BIT ERROR RATIO DETERMINATION		
Application No.:	10/773,705	Filing Date:	February 6, 2004
Examiner:	Stephen M. Baker	Group Art Unit:	2112
Docket No.:	CIS0209US	Confirmation No.	8310

Austin, Texas
December 1, 2008

Attention: Official Draftsperson
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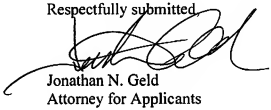
SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit six (6) sheets of formal drawings, consisting of Figures 1A, 1B, 1C, 2, 3, 4a and 4b in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (512) 439-5090.

Respectfully submitted,



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